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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **19 / 08 / 2025** | **Batch No:** | **B1** |
| **Faculty Name:** |  | **Roll No:** | **16010124080** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 2**

**Title: Binary Adders and Subtractors**

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| **Aim and Objective of the Experiment:** |
| To implement half and full adder–subtractor using gates and IC 7483 |

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| **COs to be achieved:** |
| **CO2**: Use different minimization techniques and solve combinational circuits. |

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| **Tools used:** |
| Trainer kits |

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| **Theory:** |
| **Adder:** The addition of two binary digits is the most basic operation performed by the digital computer. There are two types of adder:   * Half adder * Full adder   **Half Adder:** Half adder is a combinational logic circuit with two inputs and two outputs. It is the basic building block for the addition of two single-bit numbers.  **Full adder:** A half adder has a provision not to add a carry coming from the lower order bits when multi-bit addition is performed. for this purpose, a third input terminal is added and this circuit is to add A, B, and C where A and B are the nth order bits of the number A and B respectively and C is the carry generated from the addition of (n-1) order bits. This circuit is referred to as full adder.  **Subtractor:** Subtraction of two binary digits is one of the most basic operations performed by digital computer .there are two types of subtractors:   * Half subtractor * Full subtractor   **Half subtractor:** Logic circuit for the subtraction of B from A where A,B are 1 bit numbers is referred to as half subtract or .the subtract or process has two input and difference and borrow are the two outputs.  **Full subtractor:** As in the case of the addition using logic gates, a full subtractor is made by combining two half-sub tractors and an additional OR-gate. A full subtractor has the borrow in capability (denoted as BORIN) and so allows cascading which results in the possibility of multi-bit subtraction.  **IC 7483**  For subtraction of one binary number from another, we do so by adding 2’s complement of the former to the latter number using a full adder circuit.  IC 7483 is a 16 pin, 4-bit full adder. This IC has a provision to add the carry output to transfer and end around carry output using Co and C4 respectively.  **2’s complement:** 2’s complement of any binary no. can be obtained by adding 1 in 1’scomplement of that no.  e.g. 2’s complement of +(10)10 =1010is   |  |  |  |  | | --- | --- | --- | --- | | 1C of 1010 |  | | 0101 | |  |  | + | 1 | | -(10)10 |  | | 0110 |   In 2’s complement subtraction using IC 7483, we are representing negative number in 2’s complement form and then adding it with 1st number.  **Implementation Details:**  **Half Adder Block Diagram**    **Half Adder Circuit**  **Truth Table for Half Adder**   |  |  |  |  | | --- | --- | --- | --- | | **Inputs** | | **Outputs** | | | **A** | **B** | **A (sum)** | **B (carry)** | | 0 | 0 | 0 | 0 | | 0 | 1 | 1 | 0 | | 1 | 0 | 1 | 0 | | 1 | 1 | 0 | 1 |   **From the truth table (with steps):**  Sum = AB’ + BA’  = A xor B  Carry = AB  **Full Adder Block Diagram**    **Full Adder Circuit**  **Truth Table for Full Adder**    **From the truth table (with steps):**  Cout = A’BCin + AB’Cin + ABCin’ + ABCin    = AB (Cin + Cin’) + Cin (A’B + AB’)    = AB + Cin (A xor B)  Sum = A’B’Cin + AB’Cin’ + A’BCin’ + ABCin  = Cin (A’B’ + AB) + Cin’ (AB’ + A’B)  = Cin (AB + A’B’) + Cin’ (A xor B)  **Half Subtractor Block Diagram**    **Half Subtractor Circuit**  **Truth Table for Half Subtractor**   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  |  |  |  |  | | **A** | **B** | **DIFFERENCE(D)** | **BORROW(Bo)** |  | |  |  |  |  |  | | 0 | 0 | 0 | 0 |  | |  |  |  |  |  | | 0 | 1 | 1 | 1 |  | |  |  |  |  |  | | 1 | 0 | 1 | 0 |  | |  |  |  |  |  | | 1 | 1 | 0 | 0 |  | |  |  |  |  |  |   **From the truth table (with steps):**    B = A’B  D = A’B + AB’    = A xor B  **Full Subtractor Block Diagram**  **Full Subtractor Circuit**    **Truth Table for Full subtractor**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **A** | **B** | **BIN** | **D** | **BOROUT** | |  |  |  |  |  | | 0 | 0 | 0 | 0 | 0 | |  |  |  |  |  | | 0 | 0 | 1 | 1 | 1 | |  |  |  |  |  | | 0 | 1 | 0 | 1 | 1 | |  |  |  |  |  | | 0 | 1 | 1 | 0 | 1 | |  |  |  |  |  | | 1 | 0 | 0 | 1 | 0 | |  |  |  |  |  | | 1 | 0 | 1 | 0 | 0 | |  |  |  |  |  | | 1 | 1 | 0 | 0 | 0 | |  |  |  |  |  | | 1 | 1 | 1 | 1 | 1 | |  |  |  |  |  |     **From the truth table (with steps):**  D = A’B’Bin + A’BBin' + AB’Bin’ + ABBin  = Bin (AB + A’B’) + Bin’ (A’B + AB’)    = Bin (AB + A’B’) + Bin’ (A xor B)  Bout = A’B’Bin + A’BBin’ + A’BBin + ABBin  = A’B (Bin + Bin’) + Bin (AB + A’B’)  = A’B + Bin (AB + A’B’)  **Example:**   |  |  |  | | --- | --- | --- | | 1) 710 -210 = 510 | |  | | 7 |  | 0111 | | 2 |  | 0010 | | 1’C of 2 | | 1101 | |  |  | + 1 | | 2’C of 2 | | 1110 |   0111 + 1110 1 0101  **Pin Diagram IC7483**    **Adder**    **Subtractor** |
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| **Implementation Details** |
| **Procedure:**   1. Locate the IC 7483 and 4-not gates block on trainer kit. 2. Connect 1st input no. to A4-A1 input slot and 2nd (negative) no. to B4-B1 through 4-not gates (1C of 2nd no.) 3. Connect high input to Co so that it will get added with 1C of 2nd no. to get 2C. 4. Connect 4-bit output to the output indicators. 5. Switch ON the power supply and monitor the output for various input combinations. |
| **Post Lab Subjective/Objective type Questions:** |
| 1. Design a full adder using two half adders.      1. Perform the following Binary subtraction with the help of appropriate ICs:    1. 6-4   Ans: 6 = 0110 4 = 0100 -4 = 1100  6 + (-4) = 0 1 1 0  1 1 0 0  ----------  **(discard) <- 1 0 0 1 0 = 2 (Ans)**   * 1. 5-8   Ans: 5 = 0101 8 = 1000 -8 = 1000  5 + (-8) = 0 1 0 1  1 0 0 0  ----------  (no carry) <- 0 1 1 0 1 … (-ve no. Therefore, take 2’s comp of 1101)  **0011 = -3 (Ans)**   * 1. 7-9   Ans: 7 = 0111 9 = 1001 -9 = 0111  7 + (-9) = 0 1 1 1  0 1 1 1  ----------  (no carry) <- 0 1 1 1 0 … (-ve no. Therefore, take 2’s comp of 1110)  **0010 = -2 (Ans)** |

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| **Conclusion:** |
| The implementation of half and full adders using IC 7483 and basic logic gates demonstrates practical realization of binary arithmetic operations in digital circuits. While IC 7483 efficiently performs 4-bit binary addition with carry, using basic gates like XOR, AND, and OR for half and full adders provides a clear understanding of the underlying logic. This experiment highlights the modular approach of combining simple circuits to build complex systems, reinforcing the importance of adders as fundamental building blocks in digital electronics and computer architecture. |

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| **Signature of faculty in-charge with Date:** |